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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,480	01/28/2004	Norman Rubin	00100.03.0040	5073

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EXAMINER	
WANG, BEN C	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/767,480	RUBIN ET AL.	
	Examiner	Art Unit	
	Ben C. Wang	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/10/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending in this application and presented for examination.

Drawing Objections

2. The drawing is objected to because the following informalities:

The figure 5 does not contain all corresponding labels that are described in the sections of [0035] through [0038] of the specification.

Appropriate correction is required.

Specification Objections

3. The specification is objected to because the following informalities:

"the steps above 2D may be removed as dead code using the previous bit", cited in [0038], line 3, should be corrected as "the steps above 2D may be removed as dead code using the previous link" (please see Fig. 2, step 124 and Fig. 4, field 176).

Appropriate correction is required.

Claim Objections

4. Claims 8 and 14 are objected to because the following informalities:

"adding to each instruction a previous bit", claim 8, line 3, should be corrected as "adding to each instruction a previous link"; "wherein the first instruction includes previous bit and a write mask", claim 14, lines 7-8, should be corrected as "wherein the

first instruction includes previous link and a write mask" (please see Fig. 2, step 124 and Fig. 4, field 176).

Appropriate correction is required.

Claim Rejections – 35 USC § 101

5. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 8-13 are rejected under 35 U.S.C 101 because the claims are directed to non-statutory subject matter.

7. **As to claim 8**, the claim recites "receiving ; adding ...; adding ...; generating ...;", lines 2-8. There is no final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

8. **As to claim 9**, the claim recites "examining....; examining ...; determining ...; generating ...;", lines 2-3, and 5. There is no further final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

9. **As to claim 10**, the claim recites "examining, ...;", line 2. There is no further final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

10. **As to claim 11**, the claim recites "... the critical instruction is an instruction ...", line 1. There is no further final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

11. **As to claim 12**, the claim recites ".. the write mask is a multi-bit field ...", line 1. There is no further final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

12. **As to claim 13**, the claim recites ".. wherein each of plurality of instructions may be written to ...", lines 1-2. There is no further final tangible result produced from this claim (see MPEP 2106 (IV)(C)(2)).

Claim Rejections – 35 USC § 112

13. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

14. Claims 1-7, and 14-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

15. **Claim 1** recites the limitation "if no components are live, delete the first instruction from the machine code", line 10. It is unclear when there is a "yes" condition.

16. **Claim 14** recites the limitation "if no elements are live, deletes the first instruction from the machine code", line 14. It is unclear when there is a "yes" condition.

17. **Claim 19** recites the limitation "if no elements are live, deletes the first instruction from the machine code", line 20. It is unclear when there is a "yes" condition.

18. **Claims 2-7, 15-18, and 20** are also rejected for being dependent on rejected base claims.

Claim Rejections – 35 USC § 102(b)

19. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

20. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Grove et al. (hereafter 'Grove') (Patent No. 5,659,754).

21. **As to claim 1**, Grove discloses a method for static single assignment form dead code elimination (Abstract, Lines 1-16; Fig. 3; Col. 4, Line 66 through Col. 5, Line 10; Col. 15, Lines 25-57), the method comprising: examining a first instruction off of a worklist (Fig. 6, elements 134, 136, 138), wherein the first instruction includes a

previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47) and a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); examining at least one second instruction of the worklist (Fig. 6, elements 134, 136, 138), wherein the at least one second instructions are sources of the first instruction (Fig. 6, element 143) and each of the at least one second instructions include a previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47) and a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); determining if any components within a particular field are required for the at least one second instruction (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10); and if no components are live, delete the first instruction from the machine code (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10).

22. **As to claim 8**, Grove discloses a method for static single assignment form dead code elimination (Abstract, Lines 1-16; Fig. 3; Col. 4, Line 66 through Col. 5, Line 10; Col. 15, Lines 25-57) comprising: receiving a plurality of instructions (Fig. 9; Col. 9, Line 59 through Col. 10, Line 7); adding to each instruction a previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47); adding to each instruction a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); and generating a worklist by: for each of the plurality of instructions; determining if the instruction is a critical instruction (Col. 8, Lines 15-30, 36-37, 41-44, 48-54); and if the instruction is a critical instruction, writing the instructions to the worklist (Col. 8, Lines 15-24).

23. **As to claim 14**, Grove discloses an apparatus for static single assignment form dead code eliminations (Abstract; Fig. 3; Col. 4, Line 66 through Col. 5, Line 10; Col. 12, Line 57 through Col. 13, Line 18) comprising: at least one memory device storing a plurality of executable instructions (Fig. 1, elements 4, 9); and at least one processor (Fig. 1, element 3) operably coupled to the at least one memory device, operative to receive the plurality of executable instructions such that the processor, in response to the executable instructions: examines a first instruction off of a worklist (Fig. 6, elements 134, 136, 138), wherein the first instruction includes previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47) and a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); examines at least one second instruction of the machine code (Fig. 6, elements 134, 136, 138), wherein the at least one second instructions are sources of the first instruction (Fig. 6, element 143) and each of the at least one second instructions include a previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47) and a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); determines if all components within a particular field are live for the at least one second instruction (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10); and if no elements are live, deletes the first instruction from the machine code (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10).

24. **As to claim 19**, Grove discloses an apparatus for static single assignment form dead code eliminations (Abstract; Fig. 3; Col. 4, Line 66 through Col. 5, Line 10; Col. 12, Line 57 through Col. 13, Line 18) comprising: at least one memory device storing a

plurality of executable instructions (Fig. 1, elements 4, 9); and at least one processor (Fig. 1, element 3) operably coupled to the at least one memory device, operative to receive the plurality of executable instructions such that the processor, in response to the executable instructions: receives a plurality of instructions (Fig. 9; Col. 9, Line 59 through Col. 10, Line 7); adds to each instruction a previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47); adds to each instruction a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6); and generates a worklist by: for each of the plurality of instructions; determining if the instruction is a critical instruction (Col. 8, Lines 15-30, 36-37, 41-44, 48-54); and if the instruction is a critical instruction, writing the instructions to the worklist; examines a first instruction off of the worklist (Fig. 6, elements 134, 136, 138); examines at least one second instruction from the machine code (Fig. 6, elements 134, 136, 138), wherein the at least one second instructions are sources of the first instruction (Fig. 6, element 143); determines if any elements within a particular field are live for the at least one second instruction (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10); and if no elements are live, deletes the first instruction from the machine code (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10).

25. **As to claim 2**, Grove discloses the method further comprising: generating the worklist by: for each of a plurality of instructions, determining if the instruction is a critical instruction (Col. 8, Lines 15-30, 36-37, 41-44, 48-54); and if the instruction is a critical instruction, writing the instruction to the worklist (Col. 8, Lines 15-24).

26. **As to claim 3**, Grove discloses the method further comprising: setting a live bit for each component of the plurality of instructions (Fig. 7; Fig. 9; Fig. 10A; Fig. 10B, Fig. 10C; Col. 8, Lines 15-30, 48-54; Col. 10, Lines 31-34, 41-44, Lines 55-57).

27. **As to claim 15**, Grove discloses the apparatus wherein the at least one processor (Fig. 1, element 3) further in response to the executable instructions: generates the worklist by: for each of a plurality of instructions, determining if the instruction is a critical instruction (Col. 8, Lines 15-30, 36-37, 41-44, 48-54); and if the instruction is a critical instruction, writing the instruction to the worklist (Col. 8, Lines 15-24); sets a live bit for each component of the plurality of instructions (Fig. 7; Fig. 9; Fig. 10A; Fig. 10B, Fig. 10C; Col. 8, Lines 15-30, 48-54; Col. 10, Lines 31-34, 41-44, 55-57).

28. **As to claims 4, 11 and 16**, Grove discloses the method wherein the critical instruction is an instruction that generates an export value (Col. 8, Lines 15-30, 36-37, 41-44, 48-54).

29. **As to claims 5 and 17**, Grove discloses the method further comprising: prior to generating the worklist: receiving a plurality of instructions (Fig. 9; Col. 9, Line 59 through Col. 10, Line 7); adding to each instruction a previous link (Fig. 6, elements 133, 142, 143; Abstract, Lines 11-12; Col. 7, Lines 44-47); and adding to each instruction a write mask (Fig. 6, element 134; Col. 7, Lines 40-47; Col. 16, Lines 4-6).

30. **As to claims 6 and 12**, Grove discloses the method wherein the write mask is a multi-bit field representing a number of components in a superword register (Col. 1, Lines 7, 10; Col. 15, Lines 25-57; Col. 16, Lines 7-56)

31. **As to claims 7 and 13**, Grove discloses the method wherein each of the plurality of instructions may be written to the worklist a predetermined number of times, wherein the predetermined number of times is based on the number of components in the superword register (Col. 1, Lines 7, 10; Col. 15, Lines 16-19, 25-57; Col. 16, Lines 4-6, 7-56).

32. **As to claim 9**, Grove discloses the method further comprising: examining a first instruction off of the worklist (Fig. 6, elements 134, 136, 138); examining at least one second instruction in the machine code (Fig. 6, elements 134, 136, 138), wherein the at least one second instructions are sources of the first instruction (Fig. 6, element 143); determining if all elements within a particular field are live for the at least one second instruction (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10); and if no elements are live, deleting the first instruction from the worklist (Fig. 3; Col. 4, Line 66 through Col. 5, Line 10).

33. **As to claim 10**, Grove discloses the method of comprising: prior to examining the first instruction off of the worklist (Fig. 6, elements 134, 136, 138), setting a live bit

for each component of the plurality of instructions on the worklist (Fig. 7; Fig. 9; Fig. 10A; Fig. 10B, Fig. 10C; Col. 8, Lines 15-30, 48-54; Col. 10, Lines 31-34, 41-44, Lines 55-57).

34. **As to claims 18 and 20**, Grove discloses the apparatus further comprising: a superword register operably coupled to the at least one processor, wherein the write mask is a multi-bit field representing a number of components in the superword register (Col. 16, Lines 4-56).

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Aizikowitz et al., *Register Allocation Method and Apparatus for Truncating Runaway Lifetimes of Program Variables in a Computer System* (Pat. No. 5,761,514).
- Chow et al., *Method, System, and Computer Program Product for Performing Register Promotion via Load and Store Placement Optimization within an Optimizing Compiler* (Pat. No. 6,128,775).
- Rau et al., *Analysis and Optimization of Array Variables in Compiler for Instruction Level Parallel Processor* (Pat. No. 5,293,631).

- Chow et al., *System and Method to Efficiently Represent Aliases and Indirect Memory Operations in Static Single Assignment Form During Compilation* (Pat. No. 5,768,596).
- Hookway et al., Method and Apparatus for Forming a Translation Unit (Pat. No. 5,842,017).
- Gilbert et al., Method of Compilation Optimization Using an N-Dimensional Template for Relocated and Replicated Alignment of Arrays in Data-Parallel Programs for Reduced Data Communication During Execution (Pat. No. 5,475,842).

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben C. Wang whose telephone number is 571-270-1240. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on 571-272-3695. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BCW

TUAN DAM
SUPERVISORY PATENT EXAMINER

January 30, 2007